PATENT
Attorney Docket No. UMI-359
Client No. 80450.0090
Express Mail No. EV331753746US

COLUMN READ AMPLIFIER POWER-GATING TECHNIQUE FOR INTEGRATED CIRCUIT MEMORY DEVICES AND THOSE DEVICES INCORPORATING EMBEDDED DYNAMIC RANDOM ACCESS MEMORY (DRAM)

CROSS REFERENCE TO RELATED PATENT APPLICATIONS

The present invention is related to, and claims priority from, United States Provisional Patent Application Ser. No. 60/500,126 filed September 4, 2003 for: "0.6V 205MHz 19.5nsec TRC 16Mb Embedded DRAM" the disclosure of which is herein specifically incorporated in its entirety by this reference. The present invention is further related to the subject matter disclosed in United States Patent Applications Serial No. [UMI-355] entitled: "Sense Amplifier Power-Gating Technique for Integrated Circuit Memory Devices and Those Devices Incorporating Embedded Dynamic Random Access Memory (DRAM)" and [UMI-360] entitled: "High Speed Power-Gating Technique for Integrated Circuit Devices Incorporating a Sleep Mode of Operation", the disclosures of which are herein specifically incorporated by this reference in its entirety.

BACKGROUND OF THE INVENTION

The present invention relates, in general, to the field of integrated circuit memory devices and those devices incorporating embedded dynamic random access memory (DRAM). More particularly, the present invention relates to a column read amplifier power-gating technique for DRAM devices and those devices incorporating embedded DRAM which incorporate a power-down (or Sleep) Mode of operation.

Many types of DRAM based devices, or integrated circuits including embedded memory arrays, are currently available including extended data out ("EDO"), synchronous DRAM ("SDRAM"), double data rate ("DDR") DRAM and the like. Regardless of configuration, the primary purpose of the DRAM is to store data. Functionally, data may be written to the memory, read from it or periodically refreshed to maintain the integrity of the stored data. In current high density designs, each DRAM memory cell comprises a pass transistor coupled to an associated capacitor that may be charged to store a value representative of either a logic level "1" or "0". Data stored in these memory cells may be read out and written to them through columns of sense amplifiers coupled to complementary bit lines interconnecting rows of these cells.

Column read amplifiers have been used in integrated memory circuits to improve the speed of reading data. For DRAMs, column read amplifiers are located adjacent to the bit line sense amplifiers and the bit lines (or sense latch nodes) are connected to the gates of a pair of transistors to control the drain-to-source current through these transistors. The sources of these transistors are generally connected to a reference voltage level of circuit ground (VSS) while their drains are connected to the sources of a pair of pass transistors. These pass transistors have their gates connected to receive a column select signal (YR) and their drains are connected to the complementary local read data lines (DR and DR bar or "DRB").

In operation, the data lines are precharged "high" to a supply voltage level (VCC). When the

column select signal YR goes "high", one of the data lines is driven "low" depending on which bit line is "high". Normally, the signal YR is at 0V (VSS) when the column in not selected and is at VCC when the column is selected.

Power-gating can be used to reduce Sleep Mode power. A conventional approach involves the addition of a large power-gating transistor between the column read amplifiers and VSS. Generally, there may be a large number (on the order of 1024 or more) of read amplifiers sharing a single power-gating transistor and more than one read amplifier would be activated at the same time (typically from 16 to 128 or more). The gate of the power-gating transistor is conventionally driven below VSS during Sleep Mode to reduce the current through the read amplifiers.

The difficulty with this approach is that in the Select Mode, the current surge through the power-gating transistor can be unacceptably large due to the fact that multiple read amplifiers switch simultaneously. This causes a voltage drop across the power-gating transistor which reduces the switching speed of the read amplifiers. Furthermore, as previously mentioned, the power-gating transistor must be made very large in an attempt to minimize this voltage drop, thereby also consuming a large amount of on-chip area.

SUMMARY OF THE INVENTION

Disclosed herein is a column read amplifier power-gating technique for DRAM devices and those devices incorporating embedded DRAM which incorporate a power-down (or Sleep) mode of operation which overcomes the deficiencies of conventional power-

gating approaches. It advantageously eliminates the need for a large, separate power-gating transistor thereby saving on-chip area yet still reduces power during Sleep Mode. In operation, instead of adding the additional power-gating device, the column select signal YR is controlled such that it is now driven below VSS during Sleep Mode when N-channel pass transistors are used. If P-channel devices are used, the YR signal is driven above a supply voltage level of VCC. In either case, this significantly reduces the current through the pass transistors and yet causes no reduction in the switching speed of the column read amplifiers.

BRIEF DESCRIPTION OF THE DRAWINGS

The aforementioned and other features and objects of the present invention and the manner of attaining them will become more apparent and the invention itself will be best understood by reference to the following description of a preferred embodiment taken in conjunction with the accompanying drawings, wherein:

Fig. 1 is a high level schematic and functional block diagram of the global and local read and write data lines of a conventional integrated circuit memory array together with a representative sense amplifier and associated non-power-gated column read and write circuitry;

Fig. 2 is a schematic illustration of a conventional column read amplifier power-gating circuit and technique for placing the amplifier in one of a Select, Deselect or Sleep Mode of operation; and

Fig. 3 is a corresponding illustration of a representative embodiment of an improved column read

amplifier and power-gating circuit in accordance with the technique of the present invention through which the column read amplifier may be placed into each of the three aforementioned states without the need for a large, separate power-gating transistor.

DESCRIPTION OF A REPRESENTATIVE EMBODIMENT

With reference now to Fig. 1, a high level schematic and functional block diagram of the global and local read and write data lines of a conventional, integrated circuit memory array 100 are shown together with a representative sense amplifier and associated non-power-gated column read and write circuitry.

The memory array 100 comprises, in pertinent part, a read/write circuit 102 which may, in a particular implementation, comprise one of eight such circuits as indicated. The read/write circuit 102 comprises a sense amplifier 104 coupled between a pair of complementary bit lines (BL and BLB). Associated with each sense amplifier 104 is a column read amplifier 106 and a column write circuit 108, the former of which will be more fully describe hereinafter.

Global write data lines 126 and 128 are selectively coupled through N-channel transistors 120 and 122 respectively to local write data lines 116 and 118 in response to a write enable (WEN) signal applied to the gate terminals of transistors 120, 122. In turn, the local write data lines 116 and 118 are selectively coupled through N-channel transistors 110 and 112 respectively to complementary bit lines BL and BLB in response to a column write (YW) signal applied to the gate terminals of transistors 110 and 112.

The complementary bit lines BL and BLB are also connected to the gate terminals of N-channel transistors 130 and 132 respectively to control their drain-to-source current. The sources of transistors 130 and 132, in this non-power-gated representation, are connected directly to VSS or circuit ground. The drain terminal of each of these two devices are respectively connected to the source terminals of N-channel transistors 134 and 136 which function as pass transistors with the column read signal (YR) being applied to their common connected gate terminals. The drain terminal of transistor 134 is connected to one of a pair of local read data lines 140 (DRB) and the drain terminal of transistor 136 is connected to local read data line 142 (DR). The local read data lines 140 and 142 are respectively couplable through N-channel transistors 144 and 148 to each of a pair of global read data lines 150 and 152 in response to a read enable (REN) signal applied to the common connected gates of transistors 144 and 146 on line 148.

In operation, the local read data lines 140, 142 are precharged "high" to a supply voltage level (VCC). When the column select signal YR goes "high" at line 138, one of the data lines 140, 142 is driven "low" depending on which bit line (BL or BLB) is "high". Normally, the signal YR is at 0V (VSS) when the column in not selected and is at VCC when the column is selected.

With reference additionally now to Fig. 2, a schematic illustration of a conventional column read amplifier power-gating circuit 200 is shown together with the conventional technique for placing the

amplifier in one of a Select, Deselect or Sleep Mode of operation.

The column read amplifier power-gating circuit 200 comprises a number (e.g. 1088 in the embodiment shown) of conventional column read amplifiers 202 in conjunction with a large, separate power-gating N-channel transistor 206 which is controlled by a power-gating signal applied to its gate terminal on line 204. As will be more fully described hereinafter, the power-gating transistor 206 serves to couple or decouple the column read amplifier 202 to VSS in accordance with the signal placed on line 204 in consonance with other signals applied to the YR input.

The drain terminal of transistor 206 defines a power-gated node 208 to which the source terminals of N-channel transistors 210 and 212 are connected. The bit lines BL and BLB are coupled to the gate terminals of transistors 210 and 212 respectively. The drain terminals of transistors 210 and 212 are respectively connected to the source terminals of N-channel pass transistors 214 and 216 which have their common connected gates coupled to receive the column read signal YR at line 218. The drain terminals of transistors 214 and 216 are respectively connected to the local read data lines DRB and DR.

In a Select Mode of operation, the conventional column read amplifier power-gating circuit 200 has a level of VCC applied to YR input 218 turning "on" transistors 214 and 216 and a concurrent VCC + 0.3V applied to the gate of power-gating transistor 206 on line 204 overdriving it "on". As previously indicated, since multiple column read amplifiers 200 switch simultaneously, the current surge through the power-gating transistor 206 is quite large, causing an

effective voltage drop across this device which serves to reduce the switching speed of the column read amplifiers 200.

In a Deselect Mode of operation, the signal on line 204 remains at a level of VCC +0.3V while the signal on YR input 218 switches to a level of 0V (VSS), turning transistors 214 and 216 "off". In a Sleep Mode of operation, the YR input remains at 0V while the signal on input 204 switches to a level of -0.3V overdriving transistor 206 "off" to reduce the current through the column read amplifiers 202.

With reference additionally now to Fig. 3, a corresponding illustration of a representative embodiment of an improved column read amplifier and power-gating circuit 300 is shown (it may be one of many) together with the technique of the present invention through which the column read amplifiers may be placed into Select, Deselect and Sleep Modes of operation without the need for a large, separate power-gating transistor.

The column read amplifier and power-gating circuits 300 of the present invention comprise a pair of N-channel transistors 302 and 304 with their sources coupled to VSS without the need for a large, separate power-gating transistor 206 (Fig. 1) or the need to separately route a power-gating signal to its gate terminal. The drain terminals of transistors 302 and 304 are respectively coupled to the source terminals of N-channel pass transistors 306 and 308 which have their gate terminals connected together to receive a column read (YR) signal in accordance with the technique of the present invention. The drain terminals of transistors 306 and 308 are respectively

connected to the local read data lines DRB and DR as indicated.

In a Select Mode of operation, a single YR signal level of VCC is applied to line 310 turning both transistors 306 and 308 "on", while in a Deselect Mode of operation, a level of 0V (VSS) is applied on line 310 turning both devices "off". In a Sleep Mode of operation, a level of -0.3V (below the level of VSS) is applied to line 310 overdriving transistors 306 and 308 "off" to significantly reduce current through these pass transistors 306, 308 and, therefore, through the column read amplifier and power-gating circuit 300. The technique of the present invention causes no reduction in the switching speed of the column read amplifier and power-gating circuit 300.

While the foregoing description and accompanying figures have contemplated the use of N-channel devices in the implementation of the technique of the present invention, it should be noted that if P-channel devices are utilized instead, then the YR signal on line 310 would be merely inverted with the column read amplifier and power-gating circuit 300 being coupled to VCC (instead of VSS) and the data lines precharged to VSS ("low") instead of to VCC.

While there have been described above the principles of the present invention in conjunction with specific circuitry and voltage levels, it is to be clearly understood that the foregoing description is made only by way of example and not as a limitation to the scope of the invention. Particularly, it is recognized that the teachings of the foregoing disclosure will suggest other modifications to those persons skilled in the relevant art. Such modifications may involve other features which are

already known per se and which may be used instead of or in addition to features already described herein. Although claims have been formulated in this application to particular combinations of features, it should be understood that the scope of the disclosure herein also includes any novel feature or any novel combination of features disclosed either explicitly or implicitly or any generalization or modification thereof which would be apparent to persons skilled in the relevant art, whether or not such relates to the same invention as presently claimed in any claim and whether or not it mitigates any or all of the same technical problems as confronted by the present invention. The applicants hereby reserve the right to formulate new claims to such features and/or combinations of such features during the prosecution of the present application or of any further application derived therefrom.

What is claimed is: